APJ ABDULKALAM TECHNOLOGICAL UNIVERSITY
08 PALAKKAD CLUSTER

SECOND SEMESTER M.TECH. DEGREE EXAMINATION APRIL 2019

Branch: Electronics & Communication Engineering   Specialization: VLSI DESIGN

08EC6312 ANALOG VLSI DESIGN

Time:3 hours   **Max.marks: 60**

Answer all six questions.

Modules 1 to 6: Part 'a' of each question is compulsory and answer either part 'b' or part 'c' of each question.

Q.no.	Module 1	Marks
1.a	At a room temperature of 300° K, what capacitor size is needed to achieve a 96 dB dynamic range in an analog circuit with maximum signal levels of 1 V rms?	**3**

Answer b or c

b	Explain the different types of noise sources in MOS transistor and resistor.	**6**
c	A large MOS transistor consists of 10 individual transistors connected in parallel . Considering 1/f noise only , what is the equivalent input voltage noise spectral density for the 10 transistors compared to that of a single transistor.	**6**

Q.no.	Module 2	Marks
2.a	Draw the low frequency model of the source follower amplifier.	**3**

Answer b or c

b	Explain the working of current sink and current source with circuit diagram. Also draw its current-voltage characteristics.	**6**
c	Evaluate the performance of a common source single stage amplifier with required sketches.	**6**

Q.no.	Module 3	Marks

3.a Define CMOS differential amplifier. **3**

Answer b or c

b Emphasize the performance of cascode & folded cascode structures with required diagrams. **6**

c Design a folded cascade opamp for the following requirement: maximum differential swing=2.4V,total power dissipation=6 mW. If all of the transistors have a channel length of 0.5µm,what is the overall voltage gain? Can the input common mode level be as low as zero? **6**

Q.no.	Module 4	Marks

4.a List the properties of a current mirror circuit. **3**

Answer b or c

b Design a 2 stage low voltage opamp to meet the specifications given below V_{DD}=2V, V_{icm}(max)=2.5V , V_{icm} (min)=1V, V_{out}(max)=1.75V , V_{out}(min)=0.5V ,GB=10MHz , Slew rate=10 V/µs phase margin=60^0 for C_L=10pF **6**

c Discuss in brief about the operations of a micropower op-amp with necessary sketches. **6**

Q.no.	Module 5	Marks

5.a Explain supply independent current with a simple circuit. **4**

Answer b or c

b Emphasize the performance of a switched capacitor integrator circuit with necessary sketches. **8**

c Discuss the operation of a cmos comparator circuit & a multiplier circuit and compare its performance with required sketches. **8**

Q.no.	Module 6	Marks

6.a Assume that a DAC uses a switched capacitor non inverting amplifier with C_1=C_2 and GB=1 MHz. Find the conversion time of an 8 bit DAC if V_{REF} is 1V. **4**

Answer b or c

b Discuss in detail about the operation of a PLL with required sketches. Why charge pump & tri-state configurations are used with a PLL design. **8**

c With neat sketches explain the operation of medium speed Analog to Digital Converter. **8**