APJ ABDULKALAM TECHNOLOGICAL UNIVERSITY

08 PALAKKAD CLUSTER

Q. P. code: VLS0819342A-I **(Pages: 3)** **Name: ……**

Reg No:…….

SECOND SEMESTER M.TECH. DEGREE EXAMINATION APRIL 2019

Branch: Electronics and Communication Engineering Specialization: VLSI DESIGN

08EC6342(A) LOW POWER VLSI DESIGN

Time:3 hours **Max.marks: 60**

Answer all six questions.

Modules 1 to 6: Part 'a' of each question is compulsory and answer either part 'b' or part 'c' of each question.

Q.no.	Module 1	Marks
1.a	Examine the severity of Moore's law in the context of VLSI era of the 21st century and the associated trend for low power IC appliances.	**3**
	Answer b or c	
b	From first principles, derive the relation for the total *Power Dissipation* in a typical dynamic CMOS circuit, with the aid of suitable assumptions and circuit diagram.	**6**
c	Investigate the usage of *SPICE Simulation* to assist Low Power VLSI Design at circuit level.	**6**

Q.no.	Module 2	Marks
2.a	Examine the need for Probabilistic power analysis in modern CMOS VLSI circuits and delve on the various Stochastic quantities that have been propounded by researchers, with emphasis on any two widely accepted quantities.	**3**
	Answer b or c	
b	Estimate with the aid of Stochastic analysis, the *Static Probability* and *Transition Density* of the Boolean function, **y=a.c+b**, given that **P(a)=0.2, P(b)=0.3,P(c)=0.4** and **D(a)=1, D(b)=2, D(c)=3**. Comment on the appropriateness of the result.	**6**
c	Investigate the *Power Estimation using Entropy* and perform the detailed analysis for a typical combinational logic system.	**6**

Q.no.	Module 3	Marks
3.a	State the principle and basic operation of *Reduced Swing Clock* as an elegant means for *Power Reduction* in *Clock Networks*.	**3**

Answer b or c

b	Describe the optimizations related to *Sizing an Inverter Chain* with the aid of an illustration and supporting analysis to validate the appropriateness of *Transistor and Gate Sizing* as an elegant technique of maintaining the *Quality* at the circuit level of the design.	**6**
c	Explain how *Logic Analysis* serves as an efficient paradigm for production of high quality CMOS chips and support the deployment of *Gate Reorganization by local structuring* with clear depiction of the transformations.	**6**

Q.no.	**Module 4**	**Marks**
4.a	State how the *Reversible logic* can be deployed efficiently for reduction of Power Dissipation in low power VLSI systems.	**3**

Answer b or c

b	Investigate the approach of *Adiabatic Computation* and describe the operations of the *Complementary Adiabatic Logic* with the help of appropriate circuit diagram and four phase operational analyses.	**6**
c	Investigate the approach of *Pass Transistors logic* and elaborate on the logic synthesis systems correlating the *Boolean Decision Diagrams*.	**6**

Q.no.	**Module 5**	**Marks**
5.a	Sketch the *Energy band representations* for the *MIS structure* under the influence of different biasing voltage.	**4**

Answer b or c

b	Analyze the *Surface Space Charge region* and *Threshold Voltage* for the *MIS structure* from first principles utilizing *Poisson's law* and *Maxwell's equations*. Justify whether presence of trapped ions in the Silicon dioxide layer has implications on the derived Charge and Voltage.	**8**
c	Investigate the *Body Effect* of Long Channel MOSFET and with the aid of supporting analyses, describe the *Sub-threshold Current* and *Sub-threshold Swing.*	**8**

Q.no.	**Module 6**	**Marks**
6.a	State the method of Estimation of *Glitching Power* with reference to associated Hazards and how the *Monte Carlo Simulation* can be deployed.	**4**

Answer b or c

b	Describe the *Low Power techniques for SRAM* with clear depiction of the constraints involved and the various viable architectures.	**8**
c	Elaborate on the *Software Power Estimation* methodologies adopted by the Industry with regard to *Gate level*, *Architecture level*, *Bus Switching Activity* and *Instruction level*.	**8**