# APJ ABDULKALAM TECHNOLOGICAL UNIVERSITY
## 08 PALAKKAD CLUSTER

### SECOND SEMESTER M.TECH. DEGREE EXAMINATION APRIL 2019

**Branch: ELECTRONICS AND COMMUNICATION ENGINEERING    Specialization: VLSI DESIGN**

### 08EC6352(B) SOC DESIGN AND VERIFICATION

**Time:3 hours**          **Max. marks: 60**

**Answer all six questions**.

**Modules 1 to 6:** Part 'a' of each question is compulsory and answer either part 'b' or part 'c' of each question.

| Q.no. | Module 1 | Marks |
|---|---|---|
| **1.a** | Analyse the design specification required in a soc design. | **3** |
| | **Answer b or c** | |
| **b** | Sketch and explain the canonical SOC design. | **6** |
| **c** | Propose the valuable steps for top-down design process in SOC. Judge the top-down design process with bottom-up design process. | **6** |

| Q.no. | Module 2 | Marks |
|---|---|---|
| **2.a** | Show that the buffer cannot be placed appropriately in the hard macros. | **3** |
| | **Answer b or c** | |
| **b** | Distinguish between soft IP and hard IP. | **6** |
| **c** | Construct the core connect block diagram and explain the basic interface issues. | **6** |

| Q.no. | Module 3 | Marks |
|---|---|---|
| **3.a** | Identify activities and tools in macro integration process. | **3** |
| | **Answer b or c** | |
| **b** | Explain the top-level macro design with an example. | **6** |

| | | |
|---|---|---|
| **c** | Construct the block diagram of SoC verification scheme and explain. Judge the verification scheme. | **6** |

| Q.no. | **Module 4** | Marks |
|---|---|---|
| **4.a** | Inspect the cycle based simulators including its features and limitations. | **3** |
| | **Answer b or c** | |
| **b** | Discuss briefly about Bottom-up verification approach. | **6** |
| **c** | Illustrate Top-down design and platform based verification approach. | **6** |

| Q.no. | **Module 5** | Marks |
|---|---|---|
| **5.a** | Construct Block-level verification flow and explain its operations briefly. | **4** |
| | **Answer b or c** | |
| **b** | Analyse how system-level design and verification flow are performed in the system verification for the system-level verification. | **8** |
| **c** | Explain in detail about STV methodology with neat diagram. | **8** |

| Q.no. | **Module 6** | Marks |
|---|---|---|
| **6.a** | Sketch the communication architecture for energy efficient systems. | **4** |
| | **Answer b or c** | |
| **b** | Illustrate overall communication architecture design methodology. | **8** |
| **c** | Estimate how design space is explored in the design of communication architecture for SOC. | **8** |