APJ ABDULKALAM TECHNOLOGICAL UNIVERSITY
08 PALAKKAD CLUSTER

Q. P. Code : VLS0819322-I **(Pages: 2)** **Name: .....**

Reg. No:.....

SECOND SEMESTER M.TECH. DEGREE EXAMINATION APRIL 2019

Branch: Electronics And Communication Engineering **Specialization:** VLSI Design

08 EC 6322 CAD OF VLSI CIRCUITS

(VLSI DESIGN)

Time:3 hours **Max. marks: 60**

Answer all six questions.

Modules 1 to 6: Part 'a' of each question is compulsory and answer either part 'b' or part 'c' of each question.

Q.no.	Module 1	Marks
1.a	Define the concepts of Place and Route.	(3)
b	Explain in detail about Layout editor tools.	(6)
	OR	
c	Discuss on the various types of Back End tools.	(6)

Q.no.	Module 2	Marks
2.a	Give a brief description on VLSI Methodologies.	(3)
b	Illustrate the VLSI Physical design Automation.	(6)
	OR	
c	Explain about Design and Fabrication of VLSI decives.	(6)

Q.no.	Module 3	Marks
3.a	Briefly explain about Verilog Basis	(3)
b	Explain about:	(6)
	i) List of ports	
	ii) Port declaration	
	iii) Port connection rules	

OR

c Investigate the Basic language concepts in VLSI Design. (6)

Q.no.	**Module 4**	**Marks**
4.a	Evaluate the dataflow modeling in NAND GATE.	(3)
b	Outline the importance of Modeling system using Verilog HDL.	(6)

OR

c	Illustrate the dataflow modeling in 4:1Multiplexer.	(6)

Q.no.	**Module 5**	**Marks**
5.a	Explain about Placement.	(4)
b	Discuss in detail about routing algorithm.	(8)

OR

c	Describe the importance of Post- layout Simulation with necessary examples.	(8)

Module 6

6.a	List out the steps for PODEM algorithm.	(4)
b	Write in detail about Automatic Test Pattern Generation.	(8)

OR

c	Illustrate Scan- based testing of sequential circuits with necessary block diagrams.	(8)