

APJ ABDULKALAM TECHNOLOGICAL UNIVERSITY
08 PALAKKAD CLUSTER

Q. P. Code :VLS0819332-I

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Name

Reg. No:

SECOND SEMESTER M.TECH. DEGREE EXAMINATION APRIL 2019

Branch: Electronics & Communication Engineering

Specialization: VLSI DESIGN

08EC6332 TESTING AND VERIFICATION OF VLSI CIRCUITS

Time:3 hours

Max.marks: 60

Answer all six questions.

Modules 1 to 6: Part 'a' of each question is compulsory and answer either part 'b' or part 'c' of each question.

Q.No	Module 1	Marks
1. A.	What is Fault dominance and Fault analysis ?	(3M)
	B. Sketch the VLSI design flow involved in testing to detect the faults involved in Combinational circuits.	(6M)
	OR	
	C. Explain any of the stuck-at-fault with suitable example.	(6M)
Q.No	Module 2	Marks
2. A.	Construct Propagation D-Cubes for Two-Input NAND Gate.	(3M)
	B. Explain in detail about D-Algorithm.	(6M)
	OR	
	C. Determine the line justification and the Propagation delay path for an exclusive AND module with two inputs.	(6M)
Q.No	Module 3	Marks
3. A.	What are the disadvantages of ATPG when compared with DFT?	(3M)
	B. Discuss on various levels of DFT Techniques.	(6M)
	OR	
	C. Explain about the classical scan based design with an example.	(6M)

Q.No	Module 4	Marks
4. A. Define Controllability		(3M)
B. Explain about the test interfacing challenges in the SCAN Design.		(6M)

OR

C. Explain the concept of Boundary scan design with Architecture	(6M)
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Q.No	Module 5	Marks
5. A. What is the purpose of verification in vlsi circuits?		(4M)
B. Sketch BIST Architecture and explain the procedural testing using this architecture.		(8M)

OR

C. What are the techniques adopted in IDDQ testing ? Explain with an example.	(8M)
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Q.No	Module 6	Marks
6. A. What are the functions of a simulator ?		(4M)
B. Explain about the analytical approach in Self Checking design with real time example.		(8M)

OR

C. Write short notes on	
(i) Timing verification with real time example	(4M)
(ii) Formal Verification with real time example	(4M)